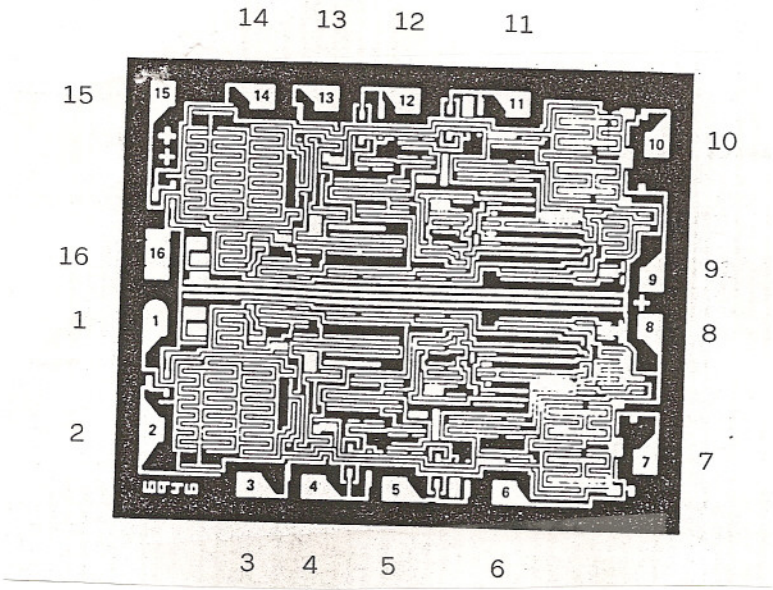
Sierra Components, Inc.

2222 Park Place • Suite 3E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD NO	FUNCTIONS
1	C_{X1}
2	$R_XC_X(1)$
3	Reset (1)
4	+TR (1)
5	−TR (1)
6	Q1
7	$\overline{Q1}$
8	V_{SS}
9	$\overline{Q2}$
10	Q2
11	−TR (2)
12	+TR (2)
13	Reset (2)
14	$R_XC_X(2)$
15	C_{X2}
16	V_{DD}

Top Material:
Backside Material:
Bond Pad Size:
Backside Potential:
Mask Ref:

APPROVED BY: MG	**DIE SIZE : 79 x 98**	**DATE: 10/23/08**
MFG: RCA	**THICKNESS:**	**P/N: CD4098BH**